CMOS Operational Amplifier Design

EECS 413 Monolithic Amplifier Circuits

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Contents

Chapter 1

Overview

This report presents the design, optimization and simulation of an operational amplifier which has to meet given specifications. Figure 1.1 gives the complete schematic of our final design. It is a simple two stages unbuffured op-amp, compensated by the capacitor C_c. This amplifier is loaded for our study by a capacitor $C_L = 2\,pF$. The first stage of the op-amp is a differential amplifier (transistors M_1, M_2, M_3, M_4, biased by transistor M_5), the second stage is an inverter (transistors M_6 and M_7). The compensation capacitor uses the Miller effect to create a dominant pole in order to stabilize the output when negative feedback is applied.

The additional transistor M_{10} is used to cancel the second pole and therefore increase the phase margin and the Unity Gain Frequency. Indeed, this transistor works in the triode region and is used as a resistor here to create a left hand plane zero that we can superpose to the second pole. As we will see, the role of the transistor M_{13} is to make sure that the voltages at node A and B are equal. We will show later how we can then choose our parameters to precisely place our zero. Note that this whole configuration (transistors M_{10}, M_{11}, M_{12}, M_{13}) replaces a simple nulling resistor R_z (we will use this notation in the following part) between B and X, but in the same time saves a lot of area. The number of transistors is not a real issue compared to the die area when we use CMOS technology.

This circuit is biased thanks to the current flowing through M_8 and mirrored in the different branches by M_{11}, M_5 and M_7. The diode connected transistors M_{91} - M_{95} take care of the needed voltage drop between V_{DD} and V_{G_8} so that the needed current flows into the drain of M_8.

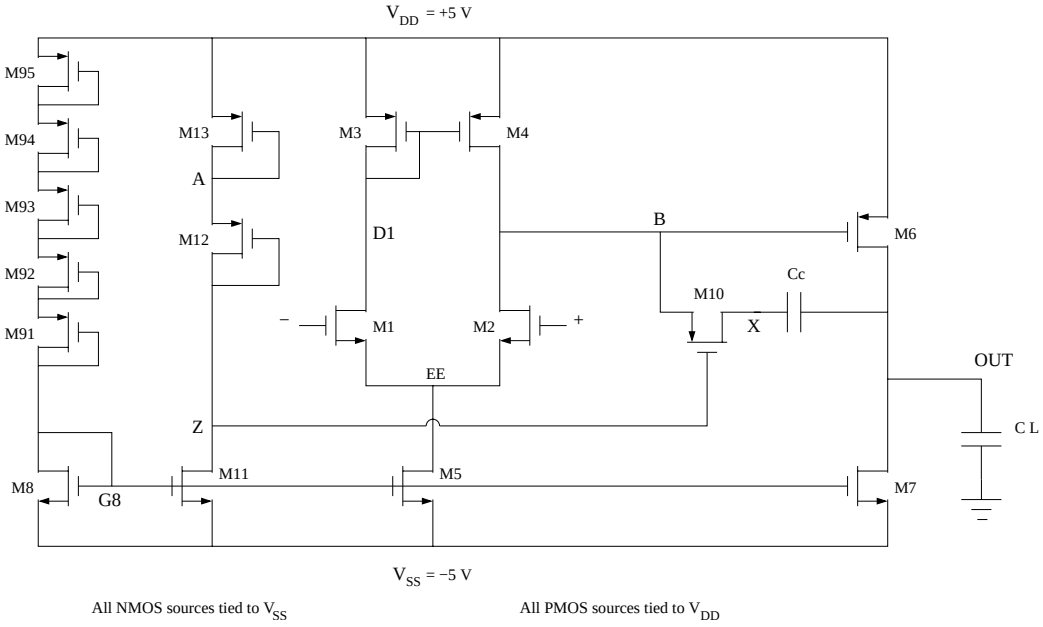

Figure 1.1: Complete Schematic of the Operational Amplifier

Chapter 2

Design

Because there was no particularly unusual specification to meet (cf. chapter 4), we chose to use the basic two stage op-amp presented. However, to increase the performances, we used first the nulling configuration presented in the overview, and secondly we optimized the design as a general geometric optimization problem. As we will see, this approach is far more efficient than the proposed traditional trial-and-error method and would permit to easily adapt the design to new specifications (however, we need to have an idea of possible values for our parameters in order to make a first guess before we run the optimization algorithm).

The most important part of the design is of course the choice of biasing points and sizes of the transistors of the two stages, the value of the capacitance C_c and the nulling of the zero. Therefore in our preliminary design, we used a perfect current source instead of the cascade of PMOS transistors $M_{91} - M_{95}$, and a simple resistor R_z instead of the whole nulling configuration around M_{10} already presented. In order to consider our problem as an optimization problem, we chose to maximize the gain, considering all the specifications as linear and nonlinear constraints. [1] note that the problem of the optimization of such a circuit is a geometric program that can therefore be treated as a good convex optimization problem. The design procedure employed was the following:

1. **Identify the independant variables**. Let us call $S_i = \frac{W_i}{L_i}$ the gate dimensions ratio for the transistor M_i. In order to simplify our design, we imposed $S_i \geq 1, \forall i$, so that we will then be able to take $L_i = 1\mu m$(minimum feature size) and $W_i \geq L_i$. The differential amplifier

has to be balanced so $S_1 = S_2$ and $S_3 = S_4$, the drain currents of M_5 and M_7 are related by $I_7 = \frac{S_7}{S_5} I_5$ and the different transistors have to match in order to cancel the offset voltage so $S_5 = \frac{2S_3S_7}{S_6}$ (see for eg. [2] $p.430$). R_z is determined after all other characteristics to place the zero correctly. Therefore we have identified 6 independant parameters for our problem: S_1, S_3, S_6, S_7, I_5, C_c.

2. **Write the specifications as constraints on these parameters**. This is where most of the work is done. We can't go here through the derivation of all the constraints, which can be found in [2], [3], and a summary in [1]. These constraints are recalled in terms of our design parameters in table 2.1, and one can find the numerical expressions of these constraints in the MATLAB input file given in appendix B. During the derivation of all the constraints, it appeared that some of them were not important and were not taken into account in the final optimization problem: for example the negative power supply rejection ratio ($PSRR^-$) is met when the $PSRR^+$ is met with usual characteristics (cf. the derivation of $PSRR^-$ and $PSRR^+$ in [3]), the positive input common mode range (CMR^+) and the DC common mode rejection ration ($CMRR$), were met as soon as the other constraints were. Critical equations were the limit on the power dissipation because it specifies important boundaries on our parameters, and the stability equation, which tells that the remaining third pole (after annulation of the second one) has to be greater than the Unity Gain Frequency (that we will denote by GB). Note that the more easily these last constraint is met, the better the final phase margin is, what stabilizes the circuit and help improve the settling time. [3] goes through the derivation of this constraint, which can be written (p_1 and p_3 are the two first remaining poles of our circuit, $A_v(0)$ is the DC gain):

$$|p_3| > A_v(0)|p_1|$$

i.e. with our parameters (C_B and C_{OUT} are the parasitic capacitances at nodes B and OUT, that we had to estimate in function of S_1,S_3,S_6,S_7, gm_1 and gm_6 are the transconductances of M_1 and M_6):

$$C_c > \left[\frac{g_{m1}}{g_{m6}} C_B C_{OUT}\right]^{0.5}$$

3. **Find an optimum point for our problem**. Trying for example to maximize the gain, we see that we have a problem of maximization under constraints. We used the `fmincon` algorithm of MATLAB to solve this problem. This is an alternative to the usual trial-and-error method, which gives good results as soon as the constraints are well specified, and offers much more flexibility. Depending on which specifications are important, we can choose to increase some constraints to match our desired result. For example here, the stability constraint was overestimated in order to get a better phase margin. Note also that the first phase margin obtained in the first design using a simple nulling resistor was more than 70^o but dropped when we changed the configuration to the one using the transistor M_{10}, at a point where I had to increase the value of C_c to $0.8\,pF$ to get a phase margin of at least 50^o. This illustrate that of course, the values given by MATLAB had to be slightly adjusted through SPICE simulations, for example in order to cancel the first existing output offset voltage. But after all, these modifications were minor.

4. **Design the desired current source**. This is pretty straightforward. We use the cascade of PMOS transistors to get the good voltage drop at the gate of M_8. The only important equation here is the one relating the drain current and the overdrive: $V_{GS} = V_t + \sqrt{\frac{2I_D}{kS}}$. The number of transistors needed and their size is estimated by hand calculation, and we adjust the desired current in M_8 with SPICE simulations.

5. **Replace R_z by the nulling transistor configuration.** The theoretical analysis can be found in [3]. Again as already mentionned, SPICE simulations had to be run to correctly adjust the zero generated, by modifying S_{10} and I_{11}.

As a conclusion, we give in table 2.1 the constraints that resulted of our analysis of the circuit. It should be noted here how important the analysis and hand calculations are to help us understand the behaviour of the circuit. These analysis were also important in the last adjustements with SPICE simulations. Note that there are some approximations due to the model used (eg. we don't take the body effect into account). This can be compensated by numerically increasing the constraints before running the algorithm and finally adjusting the values with SPICE.

Constraint	Equation
CMR^-	$\sqrt{\frac{I_5}{k_n S_1}} + \sqrt{\frac{S_6 I_5}{k_n S_3 S_7}} \leq V_{i,min} - V_{SS} - V_{t_n}$
$Output\ Voltage\ Swing^+$	$\sqrt{\frac{I_5}{k_p S_3}} \leq V_{DD} - V_{o,max}$
$Output\ Voltage\ Swing^-$	$\sqrt{\frac{S_6 I_5}{k_n S_3 S_7}} \leq V_{o,min} - V_{SS}$
$Power$	$(V_{DD} - VSS(\frac{5}{2} + \frac{S_6}{2S_3})I_5 \leq P_{max}$
$DCGain$	$\frac{4}{(\lambda_n+\lambda_p)^2 I_5}\sqrt{k_p k_n S_1 S_3} \geq A_{v,min}$
$Unity\ Gain\ Bandwidth$	$\frac{\sqrt{I_5 k_n S_1}}{C_c} \geq GB_{min}$
$SlewRate$	$\frac{I_5}{C_c} \geq SR_{min}$
$PSRR^+\,(DC)$	$\frac{S_5\sqrt{2k_n k_p}}{\lambda_n(\lambda_n+\lambda_p)I_5\sqrt{S_7}} \geq PSRR^+_{DC,min}$
$PSRR^+\,(\omega_0)$	$PSRR^{+2}_{DC}\,\frac{1}{1+\frac{4\omega_0^2 S_3 k_p C_c^2}{(\lambda_n+\lambda_p)^2\lambda_p^2 I_5^3}}$
$Stability$	$C_c > \left[\sqrt{\frac{S_1 S_3 k_n}{S_6^2 k_p}} C_B C_{OUT}\right]^{0.5}$

Table 2.1: Table of remaining important constraints after hand analysis, function of the remaining 6 variables of the design. Note that C_B and C_{OUT} were also expressed as functions of S_1,S_3,S_6,S_7 in the problem (cf. appendix B).

Chapter 3

Transistor and Bias Summary

Transistor	Dimensions $(\frac{W(\mu m)}{L(\mu m)})$	$I_D\,(\mu A)$	$V_{GS}\,(V)$	$g_m\,(\mu A/V)$	$g_0\,(\mu S)$
M_1	$\frac{100.5}{1}$	6.73	2.0915	342.7	0.153
M_2	$\frac{100.5}{1}$	6.73	2.0915	342.7	0.153
M_3	$\frac{11}{1}$	-6.73	-0.97	79	0.280
M_4	$\frac{11}{1}$	-6.73	-0.97	79	0.280
M_5	$\frac{60}{1}$	13.46	0.88	320	0.286
M_6	$\frac{73.5}{1}$	-54	-0.97	634	2.7
M_7	$\frac{230}{1}$	54	0.88	1284	1.2
M_8	$\frac{60}{1}$	12.9	0.88	306	0.263
M_{91}	$\frac{1.5}{1}$	-12.9	-1.43	41	0.548
M_{92}	$\frac{1}{1}$	-12.9	-1.79	35	0.556
M_{93}	$\frac{1.5}{1}$	-12.9	-1.86	44	0.558
M_{94}	$\frac{2}{1}$	-12.9	-1.94	51	0.560
M_{95}	$\frac{2}{1}$	-12.9	-2.09	51	0.563
M_{10} (triode)	$\frac{5.5}{1}$	0.002	-1.52	0.004	148
M_{11}	$\frac{27}{1}$	6.71	0.88	160	0.158
M_{12}	$\frac{1}{1}$	-6.71	-1.52	25	0.286
M_{13}	$\frac{11}{1}$	-6.71	-0.97	79	0.279

Table 3.1: Parameters of the Final Design. The sizes were used in the spice simulations, and to estimate the areas and perimeters of sources and drains.

Chapter 4

Performance

Parameter	Specification	Simulation
Offset Voltage	-	≈ 0
DC Gain	10000 ($80\,dB$)	125000 ($102\,dB$) at $100\,Hz$
ICMR	$[-3V; 3V]$	$[-4.08V; 4.97V]$
OVS	$[-3.5V; 3.5V]$	$[-4.994V; 4.991V]$
Total power dissipation	$\leq 1mW$	$0.87mW$
Unity Gain Frequency	$\geq 10MHz$	$56.5\,MHz$
Positive slew rate	$\geq 10V/\mu s$	$17.8V/\mu s$
Negative slew rate	$\leq -10V/\mu s$	$-13.1V/\mu s$
CMRR at DC	$\geq$ 10000 ($80\,dB$)	575000 ($115\,dB$)
$PSRR^+$ at DC	$\geq$ 10000 ($80\,dB$)	183000 ($105\,dB$)
$PSRR^-$ at DC	$\geq$ 10000 ($80\,dB$)	1.17×10^6($121\,dB$)
$PSRR^+$ at $40kHz$	$\geq$ 100 ($40\,dB$)	1748 ($66\,dB$)
$PSRR^-$ at $40kHz$	$\geq$ 100 ($40\,dB$)	32230 ($91\,dB$)
Settling time +	-	$42\,ns$ for 0.1%
Settling time -	-	$30\,ns$ for 0.1%
Phase Margin	-	51^o

Table 4.1: Performances of the designed op-amp and comparison with the desired values

Chapter 5

Discussion

It appears in table 4.1 that meeting the specification was not a real issue with this method. [1] presents the optimization method in the general case, noting that it should give the overall optimum characteristics for our parameters, as soon as one design has been chosen. However in our case, different paramaters might slightly increase the characteristics if the constraints are more finely established. For example, we see that we do not consume all the power available, what tells us that even better characteristics are possible. It should be pointed out here that changing the constraints with this method is very easy and can be done with only one line of MATLAB code, instead of redoing everything in the trial and error method. Finally, if the constraints are well studied, this method gives also a way to know when a set of constraint is not feasible with a given design. These are great advantages that justify the use of this optimization method. We will now go through the review of the characteristics of our op-amp and the methods to measure and simulate these, using HSPICE.

5.1 Offset Voltage, Power Consumption

The first thing to do is to plot the DC transfer characteristic of the op-amp in open-loop configuration. This is a way to find the eventually remaining offset. The circuit used is given in figure 5.1 and the curve in figure 5.2. We can see that theoretically an offset voltage exists of the order of $10^{-8}V$, i.e. we can neglect it (anyway we will not be able to set a real additional source for compensation with this accuracy). Note however that because of the high

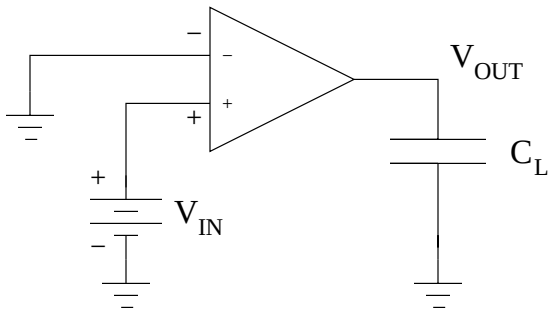

Figure 5.1: Open-loop configuration for the measure of the DC characteristic

gain of the amplifier, we have an output of around $7\,mV$ when the bases of M_1 and M_2 are both grounded.

The total power consumed by the circuit is 0.87mW. This can be found by SPICE simulation (cf. listing in annexe A) and approximated by the equation $P = (V_{DD} - V_{SS})(I_8 + I_{11} + I_5 + I_7)$.

5.2 Gain, Unity Gain Frequency, Phase Margin

All these characteristics can be visualized on the Bode diagram given in figure 5.3. This diagram was obtained by replacing the DC source of figure 5.1 by an AC source with magnitude $10\,\mu V$ and look at the frequency response: this is valid because we neglect the very small offset voltage. The low frequency gain, unity gain frequency and phase margin can be read directly on the curves. For the preparation of table 4.1, the hspice output file was also used for the determination of the low frequency gain.

5.3 Common Mode Rejection Ratio

It is also possible to evaluate directly the CMRR, as demonstrated in [3]. For this purpose, we use the circuit of figure 5.4. We can show that $\frac{V_{out}}{V_{cm}} \approx \frac{1}{CMRR}$. This allows us to plot the frequency response of the CMRR directly (using the expression builder of AWAVES), as done on figure 5.5. One can verify

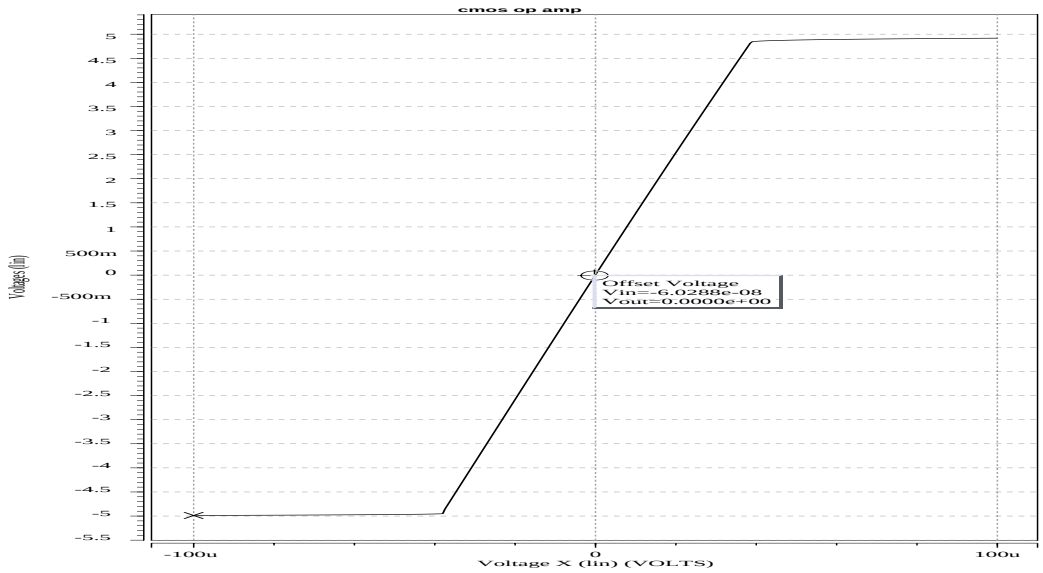

Figure 5.2: Open loop transfer characteristic of the op-amp

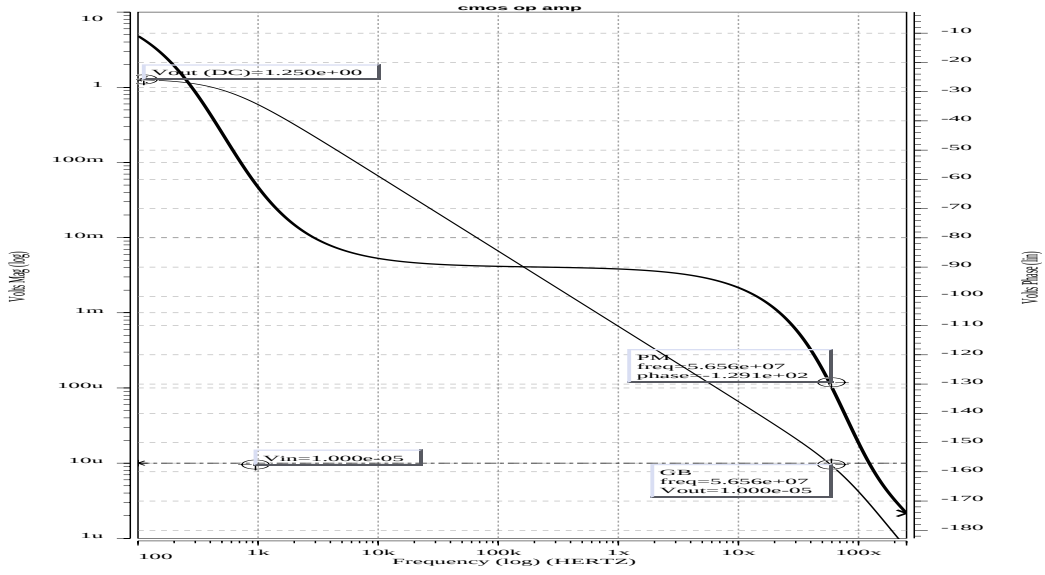

Figure 5.3: Bode diagram of the op-amp in open loop configuration.

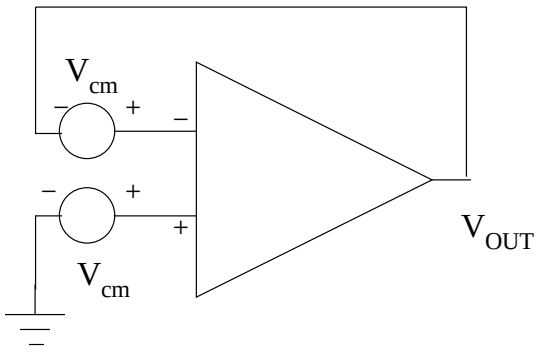

Figure 5.4: Configuration for direct measurement of CMRR.

that the specification is largely met and note that the CMRR remains high for frequencies up to $100\,kHz$.

5.4 Power Supply Rejection Ratio

To measure the $PSRR^+$ and $PSRR^-$, we insert a small sinusoidal voltage source in series with V_{DD} or V_{SS}. Note that figure 5.6 shows both additional sources connected although we performed two independant analysis and therefore connected only one source for each simulation. With this circuit, we can plot the PSRR which is given by: $\frac{V_{out}}{V_{dd}} = \frac{1}{PSRR^+}$ and $\frac{V_{out}}{V_{ss}} = \frac{1}{PSRR^-}$. The curves of figure 5.7 corresponds to this PSRR, and we can see that the specifications at DC and 40kHz are easily met.

5.5 Input Common Mode Range, Voltage Output Swing

These two parameters are determined by the fact that we want the transistors to work in the saturation region over a given range of input and output values. To measure the ICMR, we use the op-amp in a unity gain feedback configuration, whereas to measure the OVS, we use a configuration of higher gain (in our example, we used an inverter with a gain of approximately 10). Both transfer curves present a linear part which is limited by the ICMR and the OVS respectively (cf. figure 5.8). For the ICMR however, looking at the

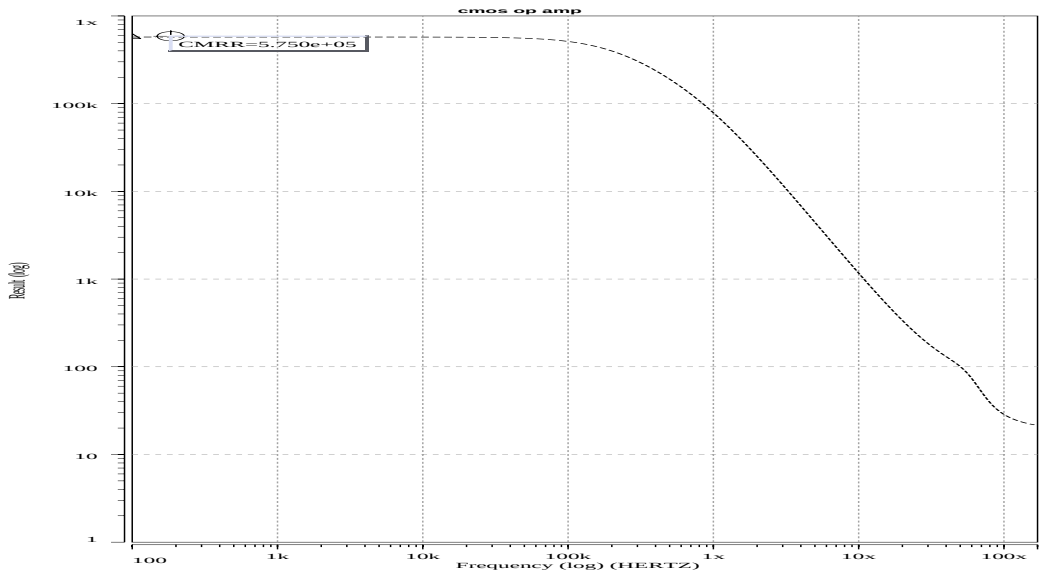

Figure 5.5: CMRR Frequency response of the Op-Amp.

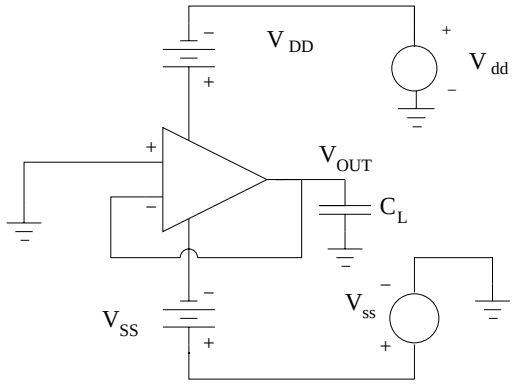

Figure 5.6: Configuration for the measurement of the PSRR.

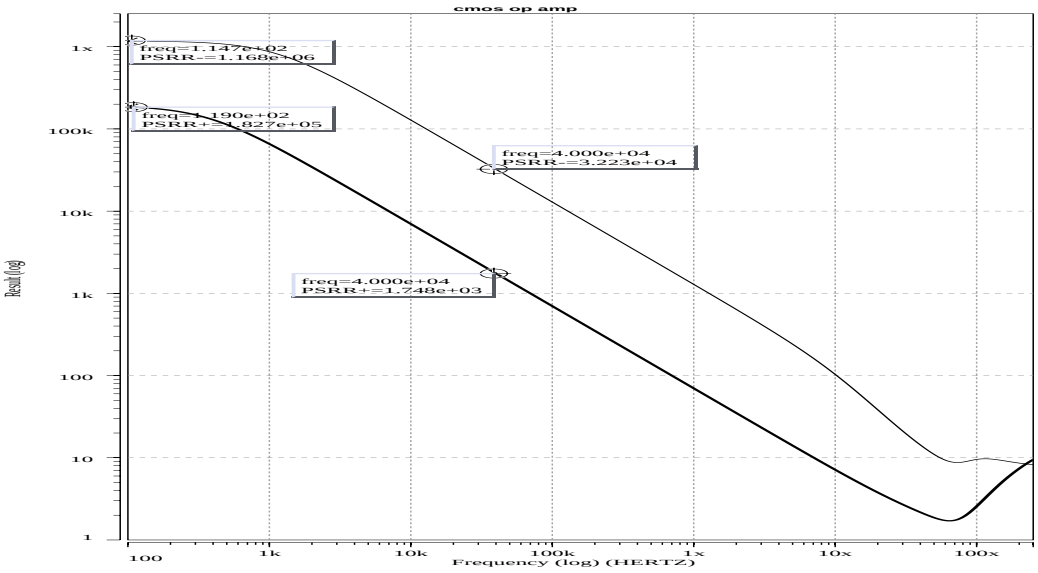

Figure 5.7: Frequency response for the positive and negative PSRR.

current flowing through M_1 is a preciser way to determine the bounds of the different regions. We used the values given on the curve to prepare table 4.1, and we can see that again we are far above the desired specifications.

5.6 Slew Rate and Settling Time

The measurement of both these parameters is made with the unity gain configuration given in figure 5.8. Applying a step at the input (gate of M_2), we want to know how fast the output voltage follows this new input voltage. The only difference in the two experiment is that we used a big voltage step for the measurement of the slew rate ($-3\,V/3\,V$) and a smaller step for the measurement of the settling time, so that the output doesn't slew. The positive and negative slew rates are given by the slopes of the response curves in figure 5.11. Note that we clearly see the influence of the parasitic capacitance of M_5, as discussed in the course, that creates the step for the positive response and decreases the negative slew rate. The specification of the SR is met, although clearly less easily than the other specifications. We

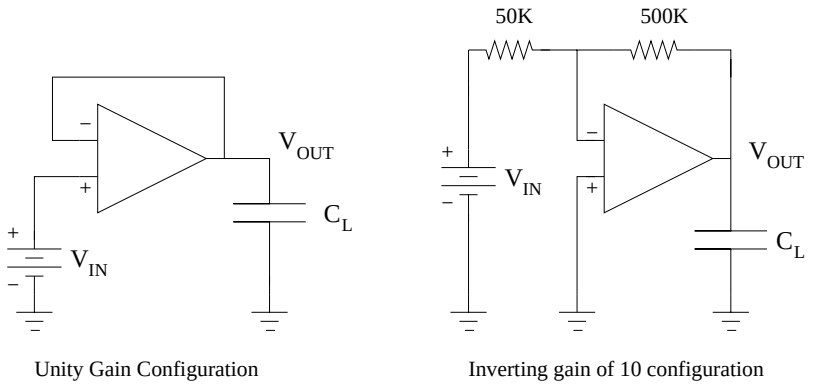

Figure 5.8: Feedback configurations used for the measure of ICMR and OVS

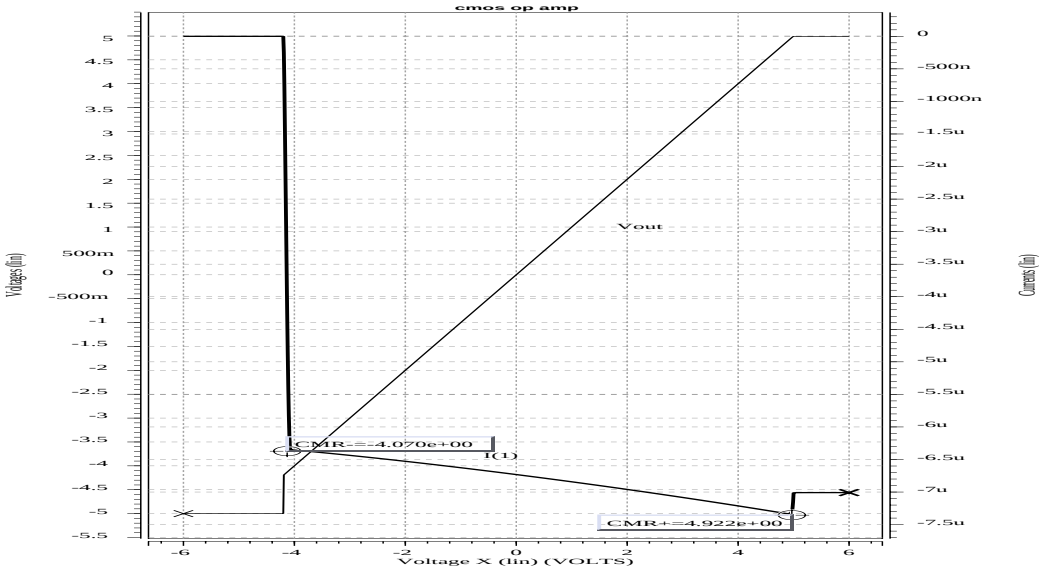

Figure 5.9: Measure of the input common mode range

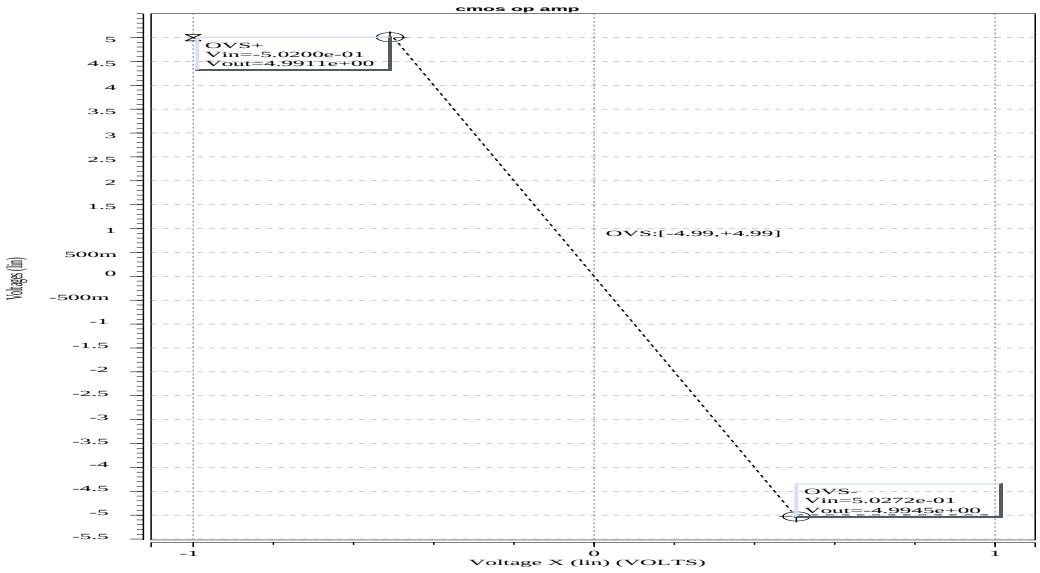

Figure 5.10: Measure of the output voltage swing

measure for the settling time the time necessary for the output to reach his final value with a 0.1% error.

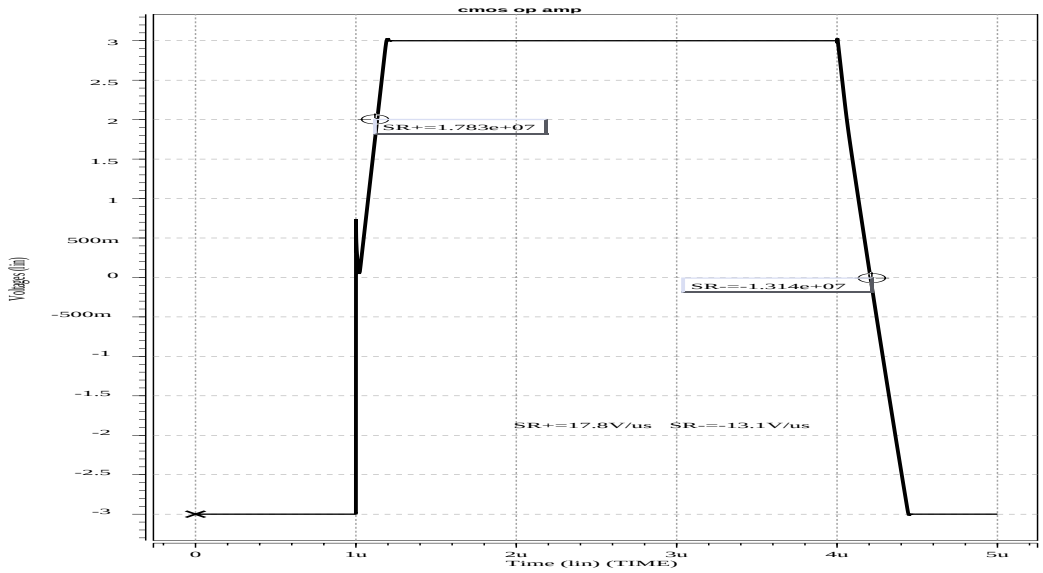

Figure 5.11: Measure of the Slew Rate of the Op-Amp.

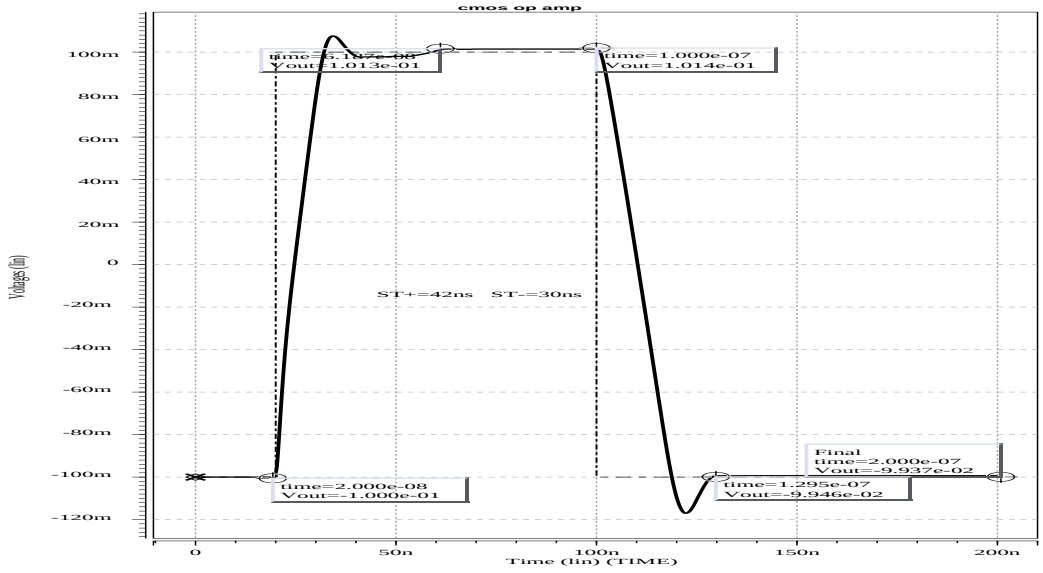

Figure 5.12: Measure of the settling time of the Op-Amp.

Conclusion

Designing an operational amplifier was a good way to get an in-depth understanding of the behaviour of these circuits, and served as an example to show that the complete elaboration of an op-amp goes far beyond what the simply small signal analysis usually explains. It is shown here how crucial for the final performances the choice of operation points, sizes of transistors, is: the initial guess used before the optimization algorithm did not meet the specifications, to be compared with the excellent performances with respect to the desired values that we finally get. That is, after one gets a good idea for a design there is still a lot of work to accomplish.

Concerning this later part of the work, two things should be emphasized here. The first one is that we saw that the CMOS technology offers a lot of flexibility through the choice of sizes, and through the fact that we can relatively independantly develop different part of the circuit, thanks to the infinite input resistance of the gates. The second point explains why we chose to use a relatively standard and not exotic kind of circuit : we tried here to emphasize how decisive the optimization method was in the process: trying a set of values and then redo the simulations until the specifications are met looks more like a guess and does not give a systematic optimized performance, whereas there exists today some very powerful optimization algorithm, which offers a lot of flexibility as well as an idea of the maximum specifications feasible with a given design. The use of the two stage unbuffered op-amp allows us to study precisely enough the different constraints. Finally this method proved to be efficient in that it permitted to go far beyond the given specitications. We chose to maximize the gain here and gained one order of magnitude on the desired value. The only characteristic that was still in the range of the specifiations at the end is the slew rate : this shows that the gain and the slew rate are probably the most difficult of our parameters to optimize at the same time.

This design problem was worth the effort and gave me the opportunity to do things by myself, after having looked at so many ideas involved in this field during the term. Ending with a working (although only through simulations !) circuit is probably the first satisfaction.

Appendix A

HSPICE input file for simulation of the circuit

MOS Transistor model used: LEVEL=4. All drain and source areas and perimeters estimated by the formula: $A = 3\mu m \times W$, $P = 6\mu m + 2 \times W$.

```
CMOS OP AMP

.OPTIONS LIST NODE POST
.AC DEC 100 100 250MEG
.PRINT AC V(G2) V(OUT)
.OP


********* Sources *********
VDD DD 0 DC +5V
VSS ss 0 DC -5V

Vin G2 0 AC 0.01mv


********* Diff Amp *********

M1 D1 0  EE SS NCHAN L=1u W=100.5u AD=301.5p AS=301.5p PD=207u PS=207u
M2 B  G2 EE SS NCHAN L=1u W=100.5u AD=301.5p AS=301.5p PD=207u PS=207u
M3 D1 D1 DD DD PCHAN L=1u W=11u AD=33p AS=33p PD=28u PS=28u
M4 B  D1 DD DD PCHAN L=1u W=11u AD=33p AS=33p PD=28u PS=28u
M5 EE G8 SS SS NCHAN L=1u W=60u AD=180p AS=180p PD=126u PS=126u


********* Second Stage *********

M6 OUT B  DD DD PCHAN L=1u W=73.5u AD=441p AS=441p PD=153u PS=153u
M7 OUT G8 SS SS NCHAN L=1u W=230u AD=690p AS=690p PD=466u PS=466u


********* Nulling Circuit and Compensation *********

M10 X Z  B  DD PCHAN L=1u W=5.5u AD=16.5p AS=16.5p PD=17u PS=17u
M11 Z G8 SS SS NCHAN L=1u W=27u AD=81p AS=81p PD=60u PS=60u
M12 Z Z  A  DD PCHAN L=1u W=1u AD=3p AS=3p PD=8u PS=8u
M13 A A  DD DD PCHAN L=1u W=11u AD=33p AS=33p PD=28u PS=28u
Cc X OUT 0.9p


********* Current of Reference *********

M91 P1 P1 DD DD PCHAN L=1u W=1.5u AD=4.5p AS=4.5p PD=9u PS=9u
```

```
M92 P2 P2 P1 DD PCHAN L=1u W=1u AD=3p AS=3p PD=8u PS=8u
M93 P3 P3 P2 DD PCHAN L=1u W=1.5u AD=4.5p AS=4.5p PD=9u PS=9u
M94 P4 P4 P3 DD PCHAN L=1u W=2u AD=6p AS=6p PD=10u PS=10u
M95 G8 G8 P4 DD PCHAN L=1u W=2u AD=6p AS=6p PD=10u PS=10u

M8 G8 G8 SS SS NCHAN L=1u W=60u AD=180p AS=180p PD=126u PS=126u

********* Load *********

CL OUT 0 2p



********* Models for the MOS transistors *********

.MODEL NCHAN NMOS LEVEL=4 VTO=0.8 KP=100u GAMMA=1.2 LAMBDA=0.02 TOX=200e-10 XJ=0.2u LD=0.1u
+PHI=0.76 NSUB=3.33e16 CGSO=168p CGDO=168p CJ=200u MJ=0.5 CJSW=500p MJSW=0.33

.MODEL PCHAN PMOS LEVEL=4 VTO=-0.8 KP=50u GAMMA=0.4 LAMBDA=0.04 TOX=200e-10 XJ=0.2u LD=0.1u
+PHI=0.64 NSUB=3.2e15 CGSO=168p CGDO=168p CJ=200u MJ=0.5 CJSW=500p MJSW=0.33

******************

.END
```

Appendix B

MATLAB input file for numerical optimization

```
function [x,g,S5,Rz,flag]=optig(x0)
% This function maximizes the gain under the given constraints
% x is the vector of our paramters: x=[S1 S3 S6 S7 I5 Cc]
% This function calls fmincon of the optimization toolbox (cf. MATLAB reference)

[x,g,flag]=fmincon(@gain,x0,[],[],[],[],[1 1 1 1 0 0],[1000 1000 1000 1000 100 1000],@nlcond);

% initial guess x0=[10 1 20 30 10 1]

S5=2*x(2)*x(4)/x(3);
Rz=((2+x(6))/x(6))*sqrt(x(2)/(50*10^(-12)*x(5)*x(3)^2));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [c,ceq]=nlcond(x)
% This function returns the necessary expressions for the constraints

c(1)=sqrt(x(5)/x(1))+sqrt((x(3)*x(5))/(x(2)*x(4)))-1.4;      % CMR-
c(2)=x(5)/x(2)-100;                                          % OVS+
c(3)=(x(3)*x(5))/(x(2)*x(4))-200;                            % OVS-
c(4)=-sqrt(x(1)*x(2))/x(5)+0.2;                              % GAIN
c(5)=0.4-(x(2)/x(5))*sqrt(x(4)/x(3));                        % PSRR+(DC)
c(6)=(x(2)*x(6)^2)/(x(5)^3)-0.00113;                         % PSRR+(40dB)
c(7)=10-x(5)/x(6);                                           % SR
c(8)=1.5-sqrt(x(5)*x(1))/x(6);                               % GB
c(9)=(2*x(1)*x(2)/x(3)^2)^0.25*sqrt(2*10^(-4)*(11*x(1)+12.7277*x(2)+13.2477*x(3)+60))-x(6);      % Stability
c(10)=x(5)*(3+x(3)/(2*x(2)))-98;    % Power

ceq=[];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function val=gain(x)
% Function to be minimized ((-1)*gain)
% We could choose here another specification of the circuit

val=-sqrt(x(1)*x(2))/x(5);
```

Bibliography

[1] M. del Mar Herhenson, S. P. Boyd and T. H. Lee, *Optimal Design of a CMOS Op-Amp via Geometric Programming*, IEEE trans. on CAD of integrated circuits and systems, vol.20, Jan. 2001.

[2] P.R. Gray, P.J. Hurst, S.H. Lewis, R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, fourth edition, Wiley, 2001.

[3] P.E. Allen, *CMOS Analog Circuit Design*, Holt, Rinehart & Winston, 1987.